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Kernel CXL Cache (safe) support

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With CXL Type2 devices comes CXL cache, implying CXL-capable devices to read/write to Host memory through system cache coherency infrastructure. If virtual machines want to take advantage of this functionality the kernel needs to properly configure the system for avoiding arbitrary access from a device to Host memory not allocated to the related VM controlling such a device. While for DMA accesses the system relies on IOMMU hardware, CXL cache accesses bring new challenges. it could require changes to the current IOMMU API or maybe add another mechanism for safely supporting it.

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