Contribution ID: **199**   Type: **not specified**

Solving Pre-silicon Kernel Upstream for RISC-V First Ever

Friday 12 December 2025 17:40 (20 minutes)

Upstreaming kernel support traditionally happens only after silicon becomes available, but this approach often delays software enablement and ecosystem readiness. For the first time in the RISC-V world, we are tackling the challenge of pre-silicon kernel upstreaming—enabling Linux kernel features ahead of actual chip availability.

In this session, we will share the methodology, toolchains, and collaborative workflows that make this possible, including the use of simulation platforms, pre-silicon verification environments, and CI/CD integration for early kernel testing. Attendees will learn how these efforts accelerate software-hardware co-design, reduce bring-up cycles, and ensure that by the time silicon arrives, the kernel is already upstream-ready.

This pioneering approach not only shortens time-to-market but also sets a new model for open source hardware-software collaboration in the RISC-V ecosystem.

Key Takeaways:
- Why pre-silicon kernel upstreaming is a game-changer for RISC-V.
- The tools and processes used to validate and upstream before silicon.
- Lessons learned and best practices for collaborating with the open source community.

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Session Classification: RISC-V MC

Track Classification: RISC-V MC