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Cooperation between CPU and system level cache by using MPAM

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MPAM (Memory System Resource Partitioning and Monitoring) enables fine-grained control over shared resources such as CPU caches, memory bandwidth, and interconnect bandwidth. In a typical memory hierarchy, the data path looks like this:
CPU(L2/L3) → NoC → SLC → DDR
This structure includes System Level Cache between CPU and DDR memory. So how to make SLC more efficient?
MPAM will assign PartID tags to data transaction. However, some MSCs such as SLC do not natively support these tags. Therefore, a mechanism is required to enable SLC to leverage the adjustments made by MPAM. This mechanism would allow tasks to be allocated to SLC based on these tags, enabling performance and energy efficiency improvements as needed.

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